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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,639	11/13/2003	Stephan Bolz	071308.0486	8974

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,639	BOLZ ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: it is suggest to change "signals" in line 3 to --signal--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1 and 18, the recitation of "can" in line 8 is indefinite because it is not a positive recitation. It is suggested to change "can flow" to --flows--.

In claim 3, the recitation of "the current mirror resistor" in lines 4-5 lacks proper antecedent basis.

In claim 6, the recitation of "the first current mirror resistor", "the second current mirror resistor" lacks proper antecedent basis.

In claim 10, the recitation of "the first current mirror resistor" in line 2 , "the current mirror input" in line 3 lacks proper antecedent basis.

In claim 11, the recitation of "the low voltage source" in line 2 lacks proper antecedent basis.

In claim 14, the recitation of "a third switching means transistor" lacks proper antecedent basis because there is no second switching means transistor recited in claim 1.

In claims 17 and 20, the recitation of "a third switching means transistor" lacks proper antecedent basis because there is no second switching means transistor recited in claims 1 and 5.

Claims 2, 4-5, 7-9, 12-13, 16 and 19 are indefinite because of the technical deficiencies of claims 1 and 18.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited prior art figure 2. Applicant's cited prior art figure 2 shows a circuit comprising a switching transistor (41) implemented as N channel MOS power transistor and connected to as a high side switch for connecting a load with a supply voltage (31), controllable switching means (51, 252) for applying a potential exceeding the voltage of the supply voltage source to the gate electrode of the switching transistor, wherein said switching means incorporate at least a first transistor switching means transistor (252) whose collector current flows at least in part to the gate electrode of the switching during ON state, and wherein the first switching means transistor is connected a current source as called for in claims 1 and 18.

5. Claims 1, 11, 14, 18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant's cited prior art figure 3. Applicant's cited prior art figure 3 shows a circuit comprising

a switching transistor (41) implemented as N channel MOS power transistor and connected to as a high side switch for connecting a load with a supply voltage (331), controllable switching means (51, 352, 353) for applying a potential exceeding the voltage of the supply voltage source to the gate electrode of the switching transistor, wherein said switching means incorporate at least a first transistor switching means transistor (51) whose collector current flows at least in part to the gate electrode of the switching during ON state, and wherein the first switching means transistor is connected a current source as called for in claims 1 and 18.

Regarding claim 11, a bootstrap capacitor (380) is provided which is connected to the low voltage source (33) on the one hand and to the source electrode (11) of the switching transistor on the other.

Regarding claims 14 and 20, a third switching transistor (351) is provided whose emitter electrode is connected to the gate electrode of the switching transistor and whose collector electrode is connected via a leakage resistor (363) to the source electrode of the switching transistor (11).

6. Claims 1-2 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Pulvirenti et al. (USP 5,656,969). Figure 3 of Pulvirenti et al. shows a circuit comprising a switching transistor (PW1) implemented as N channel MOS power transistor and connected to as a high side switch for connecting a load with a supply voltage (Vs), controllable switching means (N1,N2, mirror 1, mirror 2, mirror 3) for applying a potential exceeding the voltage of the supply voltage source to the gate electrode of the switching transistor, wherein said switching means incorporate at least a first transistor switching means transistor (N2) whose collector current

flows at least in part to the gate electrode of the switching during ON state, and wherein the first switching means transistor is connected a current source as called for in claims 1 and 18.

Regarding claim 2, the first switching means transistor N2 is connected a current source (N2 is current source when it is on) is part of a current mirror circuit (mirror 2).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 4, 5, 7 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Niimi et al. (USP 6,625,516). Figure 2 of Niimi et al. shows a circuit comprising a switching transistor (41) implemented as N channel MOS power transistor and connected to as a high side switch for connecting a load with a supply voltage (VB), controllable switching means (21, 23, 27) for applying a potential exceeding the voltage of the supply voltage source (VCP) to the gate electrode of the switching transistor, wherein said switching means incorporate at least a first transistor switching means transistor (23) whose collector current flows at least in part to the gate electrode of the switching during ON state, and wherein the first switching means transistor is connected a current source as called for in claims 1 and 18.

Regarding claim 2, the first switching means transistor connected as a current source is part of a current mirror circuit (21, 23).

Regarding claim 4, the first switching transistor 23 is pnp transistor.

Regarding claims 5 and 19, the collector current of the first switching transistor flows to the gate electrode of the switching transistor via a diode (29) connected in the flow direction.

Regarding claim 7, a second switching means is seen as transistor 27 clocked by the control signal Da.

Allowable Subject Matter

8. Claims 3, 6, 8-10, 12-13 and 15-17 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

10/14/2004